PRODUCT SPECIFICATION

nRF2401 Single Chip 2.4 GHz Radio Transceiver

Single chip 2.4 GHz Transceiver   nRF2401

FEATURES

- True single chip GFSK transceiver in a small 24-pin package (QFN24 5x5mm)
- Data rate 0 to1Mbps
- Only 2 external components
- Multi channel operation
  - 125 channels
  - Channel switching time <200μs.
  - Support frequency hopping
- Data slicer / clock recovery of data
- Address and CRC computation
- DuoCeiver™ for simultaneous dual receiver topology
- ShockBurst™ mode for ultra-low power operation and relaxed MCU performance
- Power supply range: 1.9 to 3.6 V
- Low supply current (TX), typical 10.5mA peak @ -5dBm output power
- Low supply current (RX), typical 18mA peak in receive mode
- 100% RF tested
- No need for external SAW filter
- World wide use

APPLICATIONS

- Wireless mouse, keyboard, joystick
- Keyless entry
- Wireless data communication
- Alarm and security systems
- Home automation
- Home automation
- Surveillance
- Automotive
- Telemetry
- Intelligent sports equipment
- Industrial sensors
- Toys

GENERAL DESCRIPTION

nRF2401 is a single-chip radio transceiver for the world wide 2.4 - 2.5 GHz ISM band. The transceiver consists of a fully integrated frequency synthesizer, a power amplifier, a crystal oscillator and a modulator. Output power and frequency channels are easily programmable by use of the 3-wire serial interface. Current consumption is very low, only 10.5mA at an output power of -5dBm and 18mA in receive mode. Built-in Power Down modes makes power saving easily realizable.

QUICK REFERENCE DATA

Parameter	Value	Unit
Minimum supply voltage	1.9	V
Maximum output power	0	dBm
Maximum data rate	1000	kbps
Supply current in transmit @ -5dBm output power	10.5	mA
Supply current in receive mode	18	mA
Temperature range	-40 to +85	° C
Sensitivity	-90	dBm
Supply current in Power Down mode	1	μA

Table 1 nRF2401 quick reference data

PRODUCT SPECIFICATION

nRF2401 Single Chip 2.4 GHz Radio Transceiver

Type Number	Description	Version
NRF2401 IC	24 pin QFN 5x5	A
NRF2401-EVKIT	Evaluation kit (2 test PCB, 2 configuration PCB, SW)	1.0

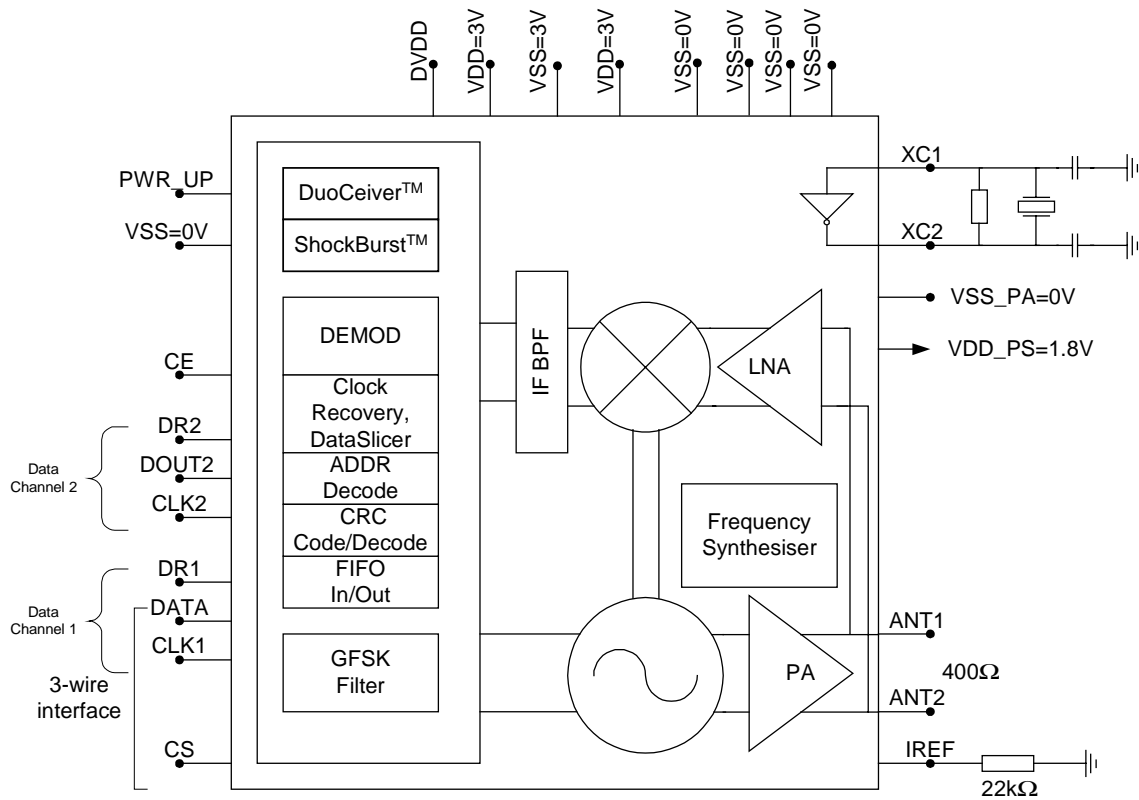Table 2 nRF2401 ordering information

BLOCK DIAGRAM

Figure 1 nRF2401 with external components.

nRF2401 Single Chip 2.4 GHz Radio Transceiver

PIN FUNCTIONS

Pin	Name	Pin function	Description
1	CE	Digital Input	Chip Enable Activates RX or TX mode
2	DR2	Digital Output	RX Data Ready at Data Channel 2 (ShockBurst™ only)
3	CLK2	Digital I/O	Clock Output/Input for RX Data Channel 2
4	DOUT2	Digital Output	RX Data Channel 2
5	CS	Digital Input	Chip Select Activates Configuration Mode
6	DR1	Digital Output	RX Data Ready at Data Channel 1 (ShockBurst™ only)
7	CLK1	Digital I/O	Clock Input (TX) & Output/Input (RX) for Data Channel 1 3-wire interface
8	DATA	Digital I/O	RX Data Channel 1/TX Data Input/ 3-wire interface
9	DVDD	Power	Positive Digital Supply output for decoupling purposes
10	VSS	Power	Ground (0V)
11	XC2	Analog Output	Crystal Pin 2
12	XC1	Analog Input	Crystal Pin 1
13	VDD_PA	Power Output	Power Supply (+1.8V) to Power Amplifier
14	ANT1	RF	Antenna interface 1
15	ANT2	RF	Antenna interface 2
16	VSS_PA	Power	Ground (0V)
17	VDD	Power	Power Supply (+3V DC)
18	VSS	Power	Ground (0V)
19	IREF	Analog Input	Reference current
20	VSS	Power	Ground (0V)
21	VDD	Power	Power Supply (+3V DC)
22	VSS	Power	Ground (0V)
23	PWR_UP	Digital Input	Power Up
24	VDD	Power	Power Supply (+3V DC)

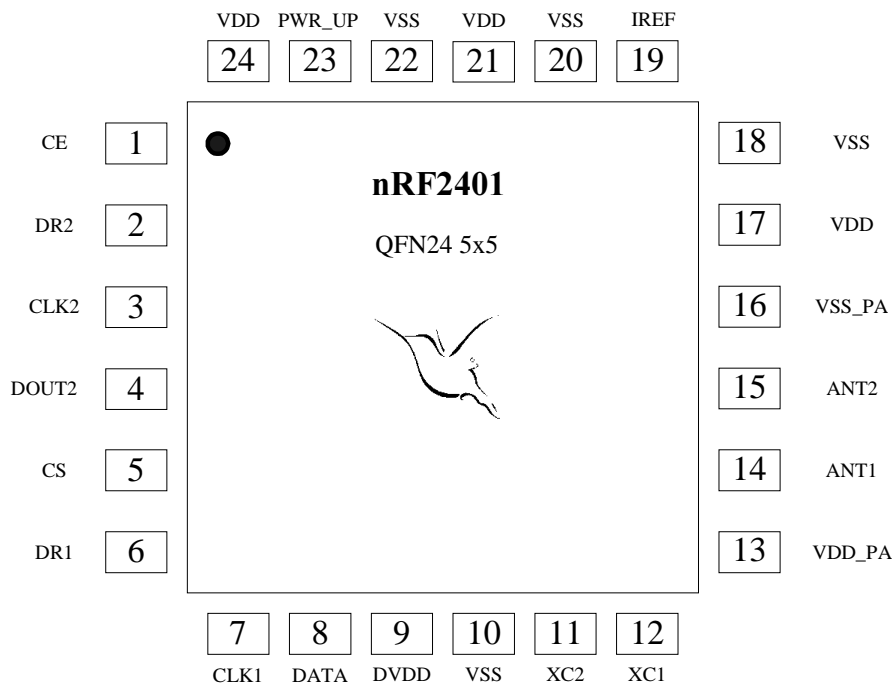Table 3 nRF2401 pin function

PIN ASSIGNMENT

Figure 2. nRF2401 pin assignment (top view) for a QFN24 5x5 package.

nRF2401 Single Chip 2.4 GHz Radio Transceiver

ELECTRICAL SPECIFICATIONS

Conditions: VDD = +3V, VSS = 0V, T_A = - 40ºC to + 85ºC

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
	Operating conditions					
VDD	Supply voltage		1.9	3.0	3.6	V
TEMP	Operating Temperature		-40	+27	+85	ºC
	Digital input pin					
V_{IH}	HIGH level input voltage		VDD- 0.3		VDD	V
V_{IL}	LOW level input voltage		Vss		0.3	V
	Digital output pin					
V_{OH}	HIGH level output voltage (I_{OH}=-0.5mA)		VDD- 0.3		VDD	V
V_{OL}	LOW level output voltage (I_{OL}=0.5mA)		Vss		0.3	V
	General RF conditions					
f_{OP}	Operating frequency	1)	2400		2524	MHz
f_{XTAL}	Crystal frequency	2)	4		20	MHz
Δf	Frequency deviation			±156		kHz
R_{GFSK}	Data rate ShockBurst™		>0		1000	kbps
R_{GFSK}	Data rate Direct Mode	3)	250		1000	kbps
$F_{CHANNEL}$	Channel spacing			1		MHz
	Transmitter operation					
P_{RF}	Maximum Output Power	4)		0	+4	dBm
P_{RFC}	RF Power Control Range		16	20		dB
P_{RFCR}	RF Power Control Range Resolution				±3	dB
P_{BW}	20dB Bandwidth for Modulated Carrier				1000	kHz
P_{RF2}	2nd Adjacent Channel Transmit Power 2MHz				-20	dBm
P_{RF3}	3rd Adjacent Channel Transmit Power 3MHz				-40	dBm
I_{VDD}	Supply current @ 0dBm output power	5)		13		mA
I_{VDD}	Supply current @ -20dBm output power	5)		8.8		mA
I_{VDD}	Average Supply current @ -5dBm output power, ShockBurst™	6)		0.8		mA
I_{VDD}	Average Supply current in stand-by mode	7)		12		μA
I_{VDD}	Average Supply current in power down			1		μA
	Receiver operation					
I_{VDD}	Supply current one channel 250kbps			18		mA
I_{VDD}	Supply current one channel 1000kbps			19		mA
I_{VDD}	Supply current two channels 250kbps			23		mA
I_{VDD}	Supply current two channels 1000kbps			25		mA
RX_{SENS}	Sensitivity at 0.1%BER (@250kbps)			-90		dBm
RX_{SENS}	Sensitivity at 0.1%BER (@1000kbps)			-80		dBm
C/I_{CO}	C/I Co-channel			6		dB
C/I_{1ST}	1st Adjacent Channel Selectivity C/I 1MHz			-1		dB
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I 2MHz			-16		dB
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I 3MHz			-26		dB
RX_B	Blocking Data Channel 2			-41		dB

1) Usable band is determined by local regulations
2) The crystal frequency may be chosen from 5 different values (4, 8, 12, 16, and 20MHz) which are specified in the configuration word, see Table 8. 16MHz are required for 1Mbps operation.
3) Data rate must be either 250kbps or 1000kbps.
4) De-embedded Antenna load impedance = 400 Ω
5) De-embedded Antenna load impedance = 400 Ω. Effective data rate 250kbps or 1Mbps.
6) De-embedded Antenna load impedance = 400 Ω. Effective data rate 10kbps.
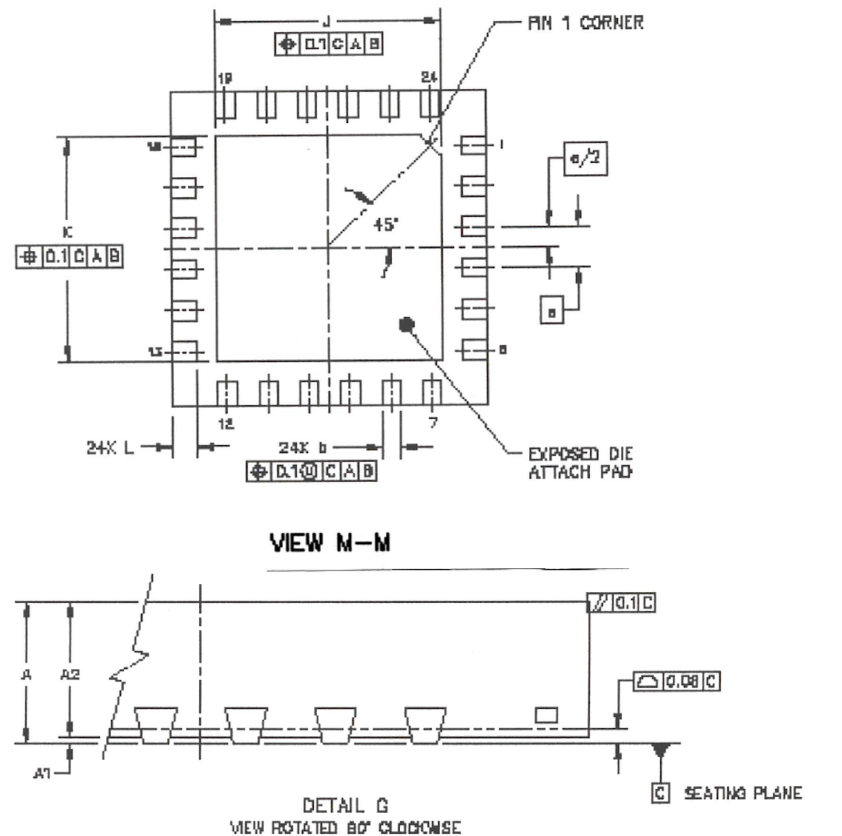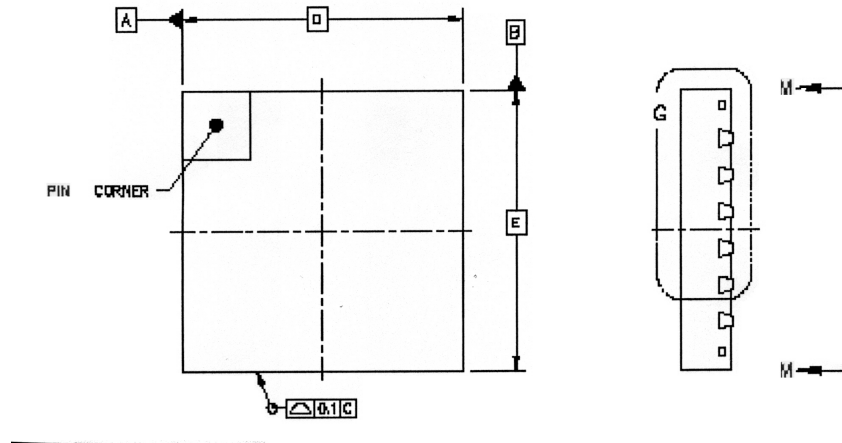7) Current if 4 MHz crystal is used.

Table 4 nRF2401 RF specifications

PACKAGE OUTLINE

nRF2401 uses the QFN 24LD 5x5 package. Dimensions are in mm.

Package Type		A	A_1	A2	b	D	E	e	J	K	L
QFN24 (5x5 mm)	Min	0.8	0.0	0.75	0.25				3.47	3.47	0.35
	typ.				0.3	5 BSC	5 BSC	0.65 BSC	3.57	3.57	0.4
	Max	1	0.05	1	0.35				3.67	3.67	0.45

Figure 3 nRF2401 package outline.

Absolute Maximum Ratings

Supply voltages
VDD ....- 0.3V to + 3.6V
VSS 0V

Input voltage
V_I ....- 0.3V to VDD + 0.3V

Output voltage
V_O ....- 0.3V to VDD + 0.3V

Total Power Dissipation
P_D (T_A=85°C).............................. 90mW

Temperatures
Operating Temperature…. - 40°C to + 85°C
Storage Temperature……. - 40°C to + 125°C

Note: Stress exceeding one or more of the limiting values may cause permanent damage to the device.

ATTENTION!
Electrostatic Sensitive Device
Observe Precaution for handling.

Glossary of Terms

Term	Description
CLK	Clock
CRC	Cyclic Redundancy Check
CS	Chip Select
CE	Chip Enable
DR	Data Ready
GFSK	Gaussian Frequency Shift Keying
ISM	Industrial-Scientific-Medical
MCU	Micro controller
OD	Overdrive
PWR_DWN	Power Down
PWR_UP	Power Up
RX	Receive
ST_BY	Standby
TX	Transmit

Table 5 Glossary

MODES OF OPERATION

Overview

The nRF2401 can be set in the following main modes depending on three control pins:

Mode	PWR_UP	CE	CS
Active (RX/TX)	1	1	0
Configuration	1	0	1
Stand by	1	0	0
Power down	0	X	X

Table 6 nRF2401 main modes

For a complete overview of the nRF2401 I/O pins in the different modes please refer to Table 7.

Active modes

The nRF2401 has two active (RX/TX) modes:

- ShockBurst™
- Direct Mode

The device functionality in these modes is decided by the content of a configuration word. This configuration word is presented in configuration section.

ShockBurst™

The ShockBurst™ technology uses on-chip FIFO to clock in data at a low data rate and transmit at a very high rate thus enabling extremely power reduction.
When operating the nRF2401 in ShockBurst™, you gain access to the high data rates (1 Mbps) offered by the 2.4 GHz band without the need of a costly, high-speed micro controller (MCU) for data processing.
By putting all high speed signal processing related to RF protocol on-chip, the nRF2401 offers the following benefits:

- Highly reduced current consumption
- Lower system cost (facilitates use of less expensive micro controller)
- Greatly reduced risk of 'on-air' collisions due to short transmission time

The nRF2401 can be programmed using a simple 3-wire interface where the data rate is decided by the speed of the micro controller.
By allowing the digital part of the application to run at low speed while maximizing the data rate on the RF link, the nRF ShockBurst™ mode reduces the average current consumption in applications considerably.

ShockBurst™ principle

When the nRF2401 is configured in ShockBurst™, TX or RX operation is conducted in the following way (10 kbps for the example only).
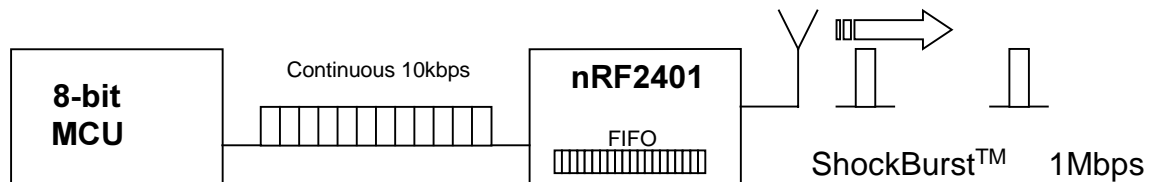

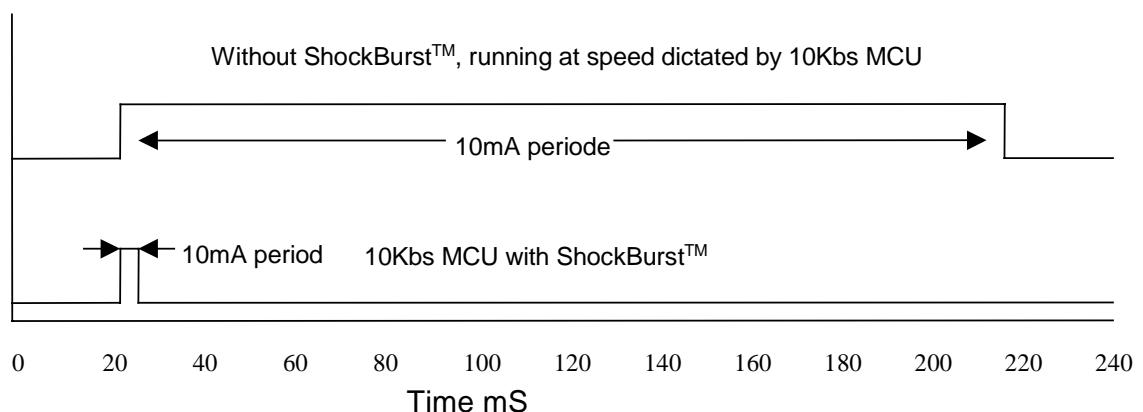Figure 4 Clocking in data with MCU and sending with ShockBurst™ technology

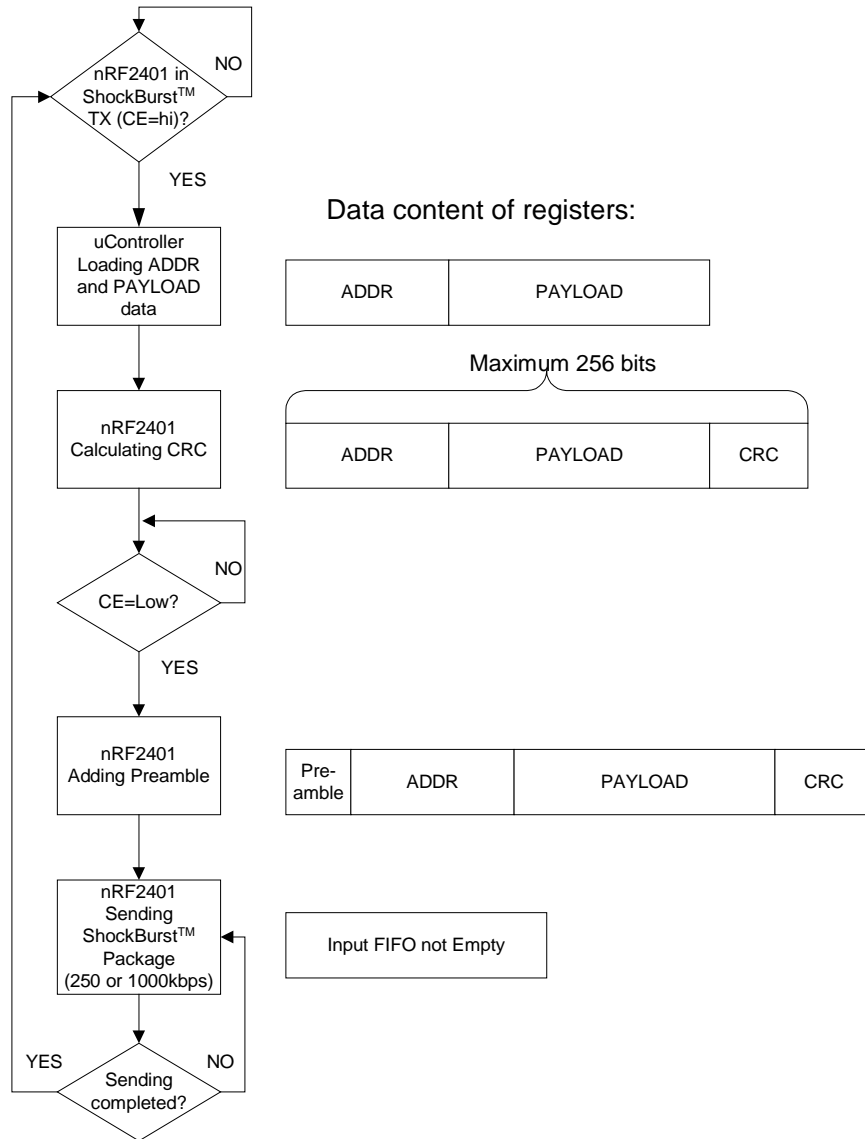Figure 5 Current consumption with & without ShockBurst™ technology

Figure 6 Flow Chart ShockBurst™ Transmit of nRF2401

nRF2401 ShockBurst™ Transmit:
MCU interface pins: CE, CLK1, DATA

1. When the application MCU has data to send, set CE high. This activates RF2401 on-board data processing.
2. The address of the receiving node (RX address) and payload data is clocked into the nRF2401. The application protocol or MCU sets the speed <1Mbps (ex: 10kbps).
3. MCU sets CE low, this activates a nRF2401 ShockBurst™ transmission.
4. nRF2401 ShockBurst™:
   - RF front end is powered up
   - RF package is completed (preamble added, CRC calculated)
   - Data is transmitted at high speed (250 kbps or 1 Mbps configured by user).
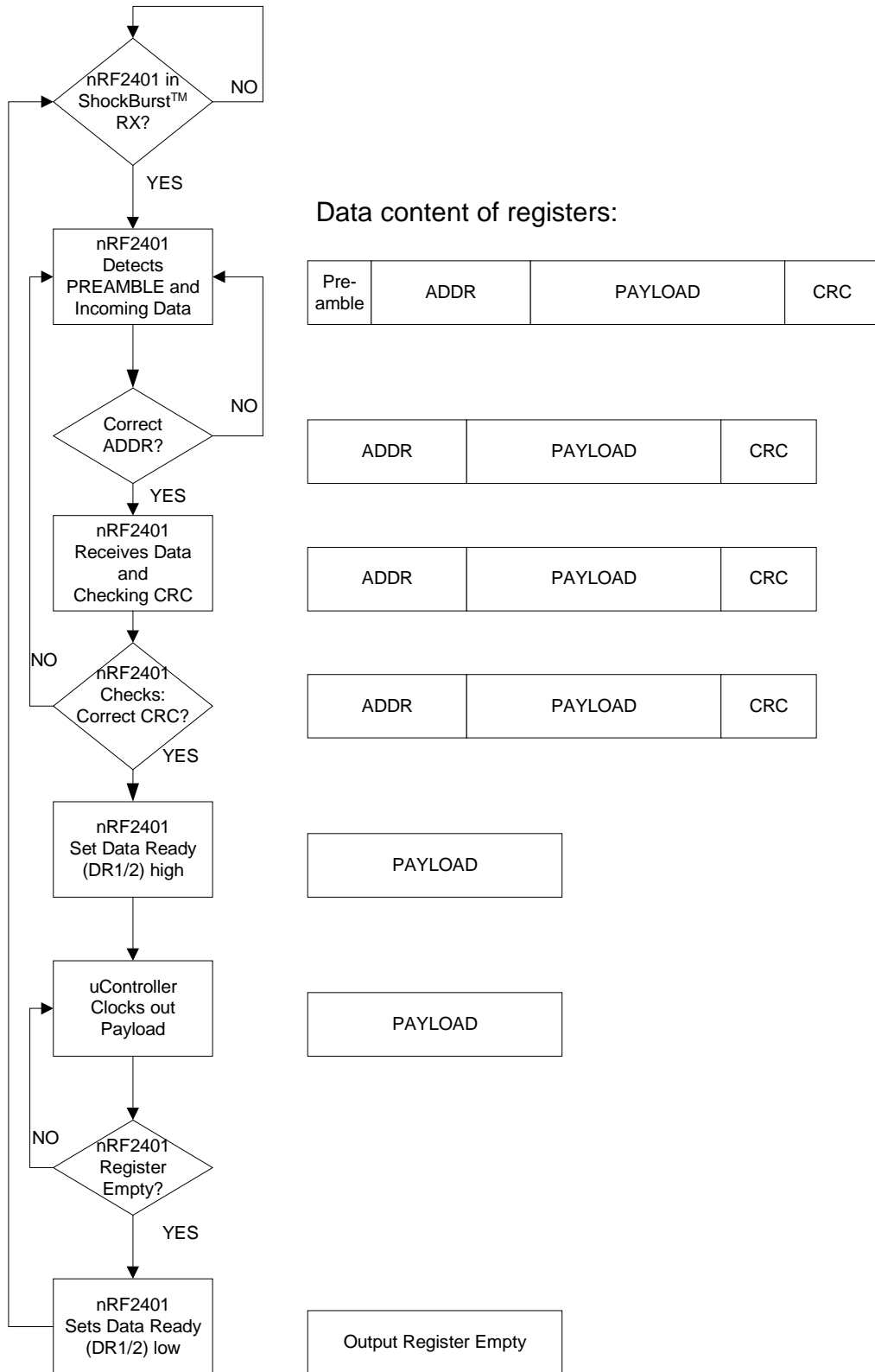   - nRF2401 return to stand-by when finished

Data content of registers:

Pre-amble	ADDR	PAYLOAD	CRC

ADDR	PAYLOAD	CRC

ADDR	PAYLOAD	CRC

ADDR	PAYLOAD	CRC

PAYLOAD

PAYLOAD

Output Register Empty

Flow chart:

- nRF2401 in ShockBurst™ RX? — NO (loop back) / YES
- nRF2401 Detects PREAMBLE and Incoming Data
- Correct ADDR? — NO (loop back) / YES
- nRF2401 Receives Data and Checking CRC
- nRF2401 Checks: Correct CRC? — NO / YES
- nRF2401 Set Data Ready (DR1/2) high
- uController Clocks out Payload
- nRF2401 Register Empty? — NO / YES
- nRF2401 Sets Data Ready (DR1/2) low

Figure 7 Flow Chart ShockBurst™ Receive of nRF2401

nRF2401 ShockBurst™ Receive:
MCU interface pins: CE, DR1, CLK1 and DATA (one RX channel receive)

1. Correct address and size of payload of incoming RF packages are set when nRF2401 is configured to ShockBurst™ RX.
2. To activate RX, set CE high.
3. After 200 µs settling, nRF2401 is monitoring the air for incoming communication.
4. When a valid package has been received (correct address and CRC found), nRF2401 removes the preamble, address and CRC bits.
5. nRF2401 then notifies (interrupts) the MCU by setting the DR1 pin high.
6. MCU may (or may not) set the CE low to disable the RF front end (low current mode).
7. The MCU will clock out just the payload data at a suitable rate (ex. 10 kbps).
8. When all payload data is retrieved nRF2401 sets DR1 low again, and is ready for new incoming data package if CE is kept high during data download. If the CE was set low, a new start up sequence can begin, see Figure 16.

Direct Mode

In direct mode the nRF2401 works like a traditional RF device. Data must be at 1Mbps, or 250kbps at low data rate setting, for the receiver to detect the signals.

Direct Mode Transmit:
MCU interface pins: CE, DATA

1. When application MCU has data to send, set CE high
2. The nRF2401 RF front end is now immediately activated, and after 200 µs settling time, data will modulate the carrier directly.
3. All RF protocol parts must hence be implemented in MCU firmware (preamble, address and CRC).

Direct Mode Receive:
MCU interface pins: CE, CLK1, and DATA

1. Once the nRF2401 is configured and powered up (CE high) in direct RX mode, DATA will start to toggle due to noise present on the air.
2. CLK1 will also start to toggle as nRF2401 is trying to lock on to the incoming data stream.
3. Once a valid preamble arrives, CLK1 and DATA will lock on to the incoming signal and the RF package will appear at the DATA pin with the same speed as it is transmitted.
4. To enable the demodulator to re-generate the clock, the preamble must be 8 bits toggling hi-low, starting with low if the first data bit low.
5. In this mode no data ready (DR) signals is available. Address and checksum verification must also be done in the receiving MC.

DuoCeiver™ Simultaneous Two Channel Receive Mode

In both ShockBurst™ & Direct modes the nRF2401 can facilitate simultaneous reception of two parallel independent frequency channels at the maximum data rate. This means:

- nRF2401 can receive data from two 1 Mbps transmitters (ex: nRF2401 or nRF2402) 8 MHz (8 frequency channels) apart through one antenna interface.
- The output from the two data channels is fed to two separate MCU interfaces.
  - Data channel 1: CLK1, DATA, and DR1
  - Data channel 2: CLK2, DOUT2, and DR2
  - DR1 and DR2 are available only in ShockBurst™.

The nRF2401 DuoCeiver™ technology provides 2 separate dedicated data channels for RX and replaces the need for two, stand alone receiver systems.
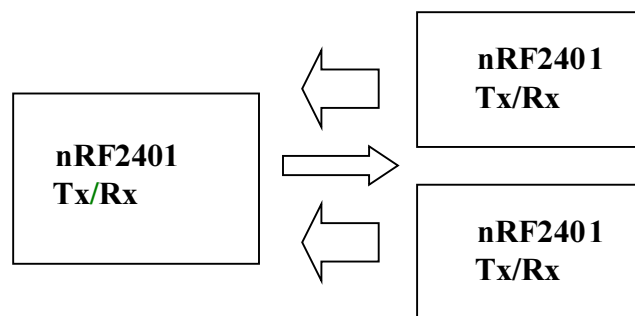

Figure 8 Simultaneous 2 channel receive on nRF2401

There is one absolute requirement for using the second data channel. For the nRF2401 to be able to receive at the second data channel the frequency channel must be 8MHz higher than the frequency of data channel 1. The nRF2401 must be programmed to receive at the frequency of data channel 1. No time multiplexing is used in nRF2401 to fulfil this function. In direct mode the MCU must be able to handle two simultaneously incoming data packets if it is not multiplexing between the two data channels. In ShockBurst™ it is possible for the MCU to clock out one data channel at a time while data on the other data channel waits for MCU availability, without any lost data packets, and by doing so reduce the needed performance of the MCU.
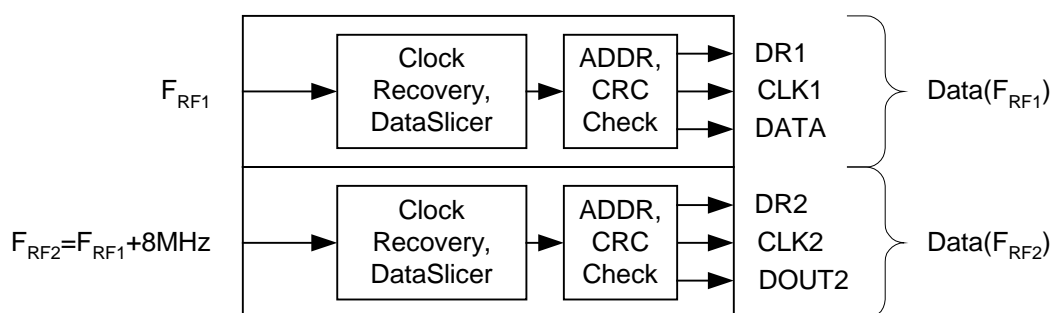

Figure 9 DuoCeiver^{TM} with two simultaneously independent receive channels.

Configuration Mode

In configuration mode a configuration word of up to 15 bytes is downloaded to nRF2401. This is done through a simple 3-wire interface (CS, CLK1 and DATA). For more information on configuration please refer to the nRF2401 Device configuration chapter on page16.

Stand-By Mode

Stand by mode is used to minimize average current consumption while maintaining short start up times. In this mode, part of the crystal oscillator is active. Current consumption is dependent on crystal frequency (Ex: 12 µA @ 4 MHz, 32 µA @ 16 MHz). The configuration word content is maintained during stand by.

Power Down Mode

In power down the nRF2401 is disabled with minimal current consumption, typically less than 1µA. Entering this mode when the device is not active minimizes average current consumption, maximizing battery lifetime. The configuration word content is maintained during power down.

nRF2401 Single Chip 2.4 GHz Radio Transceiver

Pin configuration for the different modes of nRF2401

nRF2401 MODES	INPUT PINS			BIDIR PINS			OUTPUT PINS		
	PWR_UP	CE	CS	CLK1 (direction)	DATA (direction)	CLK2 (direction)	DR1	DR2	DOUT2
Power down	0	0	X	In	In	In	0	0	0
Stand by	1	0	0	X	X	X	0	0	0
Configuration	1	0	1	In	In	In	0	0	0
TX ShockBurst™	1	1	0	In / CLK	In / CONFIG DATA	In / CLK	0	0	0
TX Direct	1	1	0	In / Set to 0	In / DATA	In / X	0	0	0
RX ShockBurst™ in one channel	1	1	0	In / CLK	Out / DATA	In / CLK	DR1	0	0
RX ShockBurst™ in two channels	1	1	0	In / CLK	Out / DATA	In / CLK	DR1	DR2	DATA
RX Direct in one channel	1	1	0	Out / CLK	Out / DATA	Out / 0	0	0	0
RX Direct in two channels	1	1	0	Out / CLK	Out / DATA	Out / CLK	DR1	DR2	DATA

Table 7 Pin configuration of nRF2401.

DEVICE CONFIGURATION

All configuration of the nRF2401 is done via a 3-wire interface to a single configuration register. The configuration word can be up to 15 bytes long for ShockBurst™ use and up to 2 bytes long for direct mode.

Configuration for ShockBurst™ operation

The configuration word in ShockBurst™ enables the nRF2401 to handle the RF protocol. Once the protocol is completed and loaded into nRF2401 only one byte, bit[7:0], needs to be updated during actual operation.

The configuration blocks dedicated to ShockBurst™ is as follows:
- Payload section width: Specifies the number of payload bits in a RF package. This enables the nRF2401 to distinguish between payload data and the CRC bytes in a received package.
- Address width: Sets the number of bits used for address in the RF package. This enables the nRF2401 to distinguish between address and payload data.
- Address (RX Channel 1 and 2): Destination address for received data.
- CRC: Enables nRF2401 on-chip CRC generation and de-coding.

NOTE:
These configuration blocks, with the exception of the CRC, are dedicated for the packages that a nRF2401 is to receive.
In TX mode, the MCU must generate an address and a payload section that fits the configuration of the nRF2401 that is to receive the data.
When using the nRF2401 on-chip CRC feature ensure that CRC is enabled and uses the same length for both the TX and RX devices.

PRE-AMBLE	ADDRESS	PAYLOAD	CRC

Figure 10 Data packet set-up

Configuration for Direct Mode operation
For direct mode operation only the two first bytes (bit[15:0]) of the configuring word are relevant.

Configuration Word overview

	Bit position	Number of bits	Name	Function
ShockBurst™ configuration	143:120	24	TEST	Reserved for testing
	119:112	8	DATA2_W	Length of data payload section RX channel 2
	111:104	8	DATA1_W	Length of data payload section RX channel 1
	103:64	40	ADDR2	Up to 5 byte address for RX channel 2
	63:24	40	ADDR1	Up to 5 byte address for RX channel 1
	23:18	6	ADDR_W	Number of address bits (both RX channels).
	17	1	CRC_L	8 or 16 bit CRC
	16	1	CRC_EN	Enable on-chip CRC generation/checking.
General device configuration	15	1	RX2_EN	Enable two channel receive mode
	14	1	CM	Communication mode (Direct or ShockBurst™)
	13	1	RFDR_SB	RF data rate (1Mbps requires 16MHz crystal)
	12:10	3	XO_F	Crystal frequency
	9:8	2	RF_PWR	RF output power
	7:1	7	RF_CH#	Frequency channel
	0	1	RXEN	RX or TX operation

Table 8 Table of configuration words.

The configuration word is shifted in MSB first on positive CLK1 edges. New configuration is enabled on the falling edge of CS.

NOTE.
On the falling edge of CS, the nRF2401 updates the number of bits actually shifted in during the last configuration.
Ex:
If the nRF2401 is to be configured for 2 channel RX in ShockBurst™, a total of 120 bits must be shifted in during the first configuration after VDD is applied.
Once the wanted protocol, modus and RF channel are set, only one bit (RXEN) is shifted in to switch between RX and TX.

Configuration Word Detailed Description

The following describes the function of the 144 bits (bit 143 = MSB) that is used to configure the nRF2401.
General Device Configuration: bit[15:0]
ShockBurst™ Configuration: bit[119:0]
Test Configuration: bit[143:120]

MSB			TEST				
D143	D142	D141	D140	D139	D138	D137	D136
Reserved for testing							
1	0	0	0	1	1	1	0	Default

MSB							TEST							Close PLL in TX
D135	D134	D133	D132	D131	D130	D129	D128	D127	D126	D125	D124	D123	D122	D121	D120
Reserved for testing														Close PLL in TX	
0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	0	Default

		DATA2_W					
D119	D118	D117	D116	D115	D114	D113	D112
Data width channel#2 in # of bits excluding addr/crc							
0	0	1	0	0	0	0	0	Default

		DATA1_W					
D111	D110	D109	D108	D107	D106	D105	D104
Data width channel#1 in # of bits excluding addr/crc							
0	0	1	0	0	0	0	0	Default

			ADDR2								
D103	D102	D101	….	D71	D70	D69	D68	D67	D66	D65	D64
Channel#2 Address RX (up to 40bit)											
0	0	0	…	1	1	1	0	0	1	1	1	Default

			ADDR1								
D63	D62	D61	….	D31	D30	D29	D28	D27	D26	D25	D24
Channel#1 Address RX (up to 40bit)											
0	0	0	…	1	1	1	0	0	1	1	1	Default

		ADDR_W			
D23	D22	D21	D20	D19	D18
Address width in # of bits (both channels)					
0	0	1	0	0	0	Default

CRC	
D17	D16
CRC Mode 1 = 16bit, 0 = 8bit	CRC 1 = enable; 0 = disable
0	1	Default

RF-Programming															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Two Ch.	BUF	OD	XO Frequency			RF Power		Channel selection							RXEN
0	0	0	0	1	1	1	1	0	0	0	0	0	1	0	0	Default

Table 9 Configuration data word

The MSB bit should be loaded first into the configuration register.
Default configuration word: h8E08.1C20.2000.0000.00E7.0000.0000.E721.0F04.

ShockBurst™ configuration:

The section B[119:16] contains the segments of the configuration register dedicated to ShockBurst™ operational protocol. After VDD is turned on ShockBurst™ configuration is done once and remains set whilst VDD is present. During operation only the first byte for frequency channel and RX/TX switching need to be changed.

PLL_CTRL

PLL_CTRL		
D121	**D120**	**PLL**
0	0	Open TX/Closed RX
0	1	Open TX/Open RX
1	0	Closed TX/Closed RX
1	1	Closed TX/Open RX

Table 10 PLL setting.

Bit 121-120:
> PLL_CTRL: Controls the setting of the PLL for test purposes. With closed PLL in TX no deviation will be present.

DATAx_W

DATA2_W							
119	118	117	116	115	114	113	112

DATA1_W							
111	110	109	108	107	106	105	104

Table 11 Number of bits in payload.

Bit 119 – 112:
> DATA2_W: Length of RF package payload section for receive-channel 2.

Bit 111 – 104:
> DATA1_W: Length of RF package payload section for receive-channel 1.

NOTE:
> The total number of bits in a ShockBurst™ RF package may not exceed 256!
> Maximum length of payload section is hence given by:

$$DATAx\_W(bits) = 256 - ADDR\_W - CRC$$

Where:
> ADDR_W: length of RX address set in configuration word B[23:18]
> CRC: check sum, 8 or 16 bits set in configuration word B[17]
> PRE: preamble, 4 or 8 bits are automatically included

Shorter address and CRC leaves more room for payload data in each package.

ADDRx

ADDR2											
103	102	101	….	71	70	69	68	67	66	65	64

ADDR1											
63	62	61	….	31	30	29	28	27	26	25	24

Table 12 Address of receiver #2 and receiver #1.

Bit 103 – 64:
ADDR2: Receiver address channel 2, up to 40 bit.

Bit 63 – 24: ADDR1
ADDR1: Receiver address channel 1, up to 40 bit.

NOTE!
Bits in ADDRx exceeding the address width set in ADDR_W are redundant and can be set to logic 0.

ADDR_W & CRC

ADDR_W						CRC_L	CRC_EN
23	22	21	20	19	18	17	16

Table 13 Number of bits reserved for RX address + CRC setting.

Bit 23 – 18:
ADDR_W: Number of bits reserved for RX address in ShockBurst™ packages.

NOTE:
Maximum number of address bits is 40 (5 bytes). Values over 40 in ADDR_W are not valid.

Bit 17:
CRC_L: CRC length to be calculated by nRF2401 in ShockBurst™.
Logic 0: 8 bit CRC
Logic 1: 16 bit CRC

Bit: 16:
CRC_EN: Enables on-chip CRC generation (TX) and verification (RX).
Logic 0: On-chip CRC generation/checking disabled
Logic 1: On-chip CRC generation/checking enabled

NOTE:
An 8 bit CRC will increase the number of payload bits possible in each ShockBurst™ data packet, but will also reduce the system integrity.

PRODUCT SPECIFICATION

General device configuration:

This section of the configuration word handles RF and device related parameters.

Modes:

RX2_EN	CM	RFDR_SB	XO_F			RF_PWR	
15	14	13	12	11	10	9	8

Table 14 RF operational settings.

Bit 15:

    RX2_EN:

        Logic 0: One channel receive

        Logic 1: Two channels receive

    NOTE:

        In two channels receive, the nRF2401 receives on two, separate frequency channels simultaneously. The frequency of receive channel 1 is set in the configuration word B[7-1], receive channel 2 is always 8 channels (8 MHz) above receive channel 1.

Bit 14:

    Communication Mode:

        Logic 0: nRF2401 operates in direct mode.

        Logic 1: nRF2401 operates in ShockBurst™ mode

Bit 13:

    RF Data Rate:

        Logic 0: 250 kbps

        Logic 1: 1 Mbps

    NOTE:

        Utilizing 250 kbps instead of 1Mbps will improve the receiver sensitivity by 10 dB. 1Mbps requires 16MHz crystal.

Bit 12-10:

    XO_F: Selects the nRF2401 crystal frequency to be used:

XO FREQUENCY SELECTION			
D12	D11	D10	Crystal Frequency [MHz]
0	0	0	4
0	0	1	8
0	1	0	12
0	1	1	16
1	0	0	20

Table 15 Crystal frequency setting.

Bit 9-8:

      RF_PWR: Sets nRF2401 RF output power in transmit mode:

RF OUTPUT POWER		
D9	D8	P [dBm]
0	0	-20
0	1	-10
1	0	-5
1	1	0

Table 16 RF output power setting.

RF channel & direction

RF_CH#							RXEN
7	6	5	4	3	2	1	0

Table 17 Frequency channel + RX / TX setting.

Bit 7 – 1:

      RF_CH#: Sets the frequency channel the nRF2401 operates on.

The channel frequency in *transmit* is given by:

$$Channel_{RF} = 2400\ MHz + RF\_CH\# \cdot 1.0\ MHz$$

      RF_CH #: between 2400MHz and 2527MHz may be set.

The channel frequency in *data channel 1* is given by:

$$Channel_{RF} = 2400\ MHz + RF\_CH\# \cdot 1.0\ MHz\ \ (Receive\ at\ PIN\#8)$$

      RF_CH #: between 2400MHz and 2524MHz may be set.

      NOTE:
      The channels above 83 can only be utilized in certain territories (ex: Japan)

The channel frequency in *data channel 2* is given by:

$$Channel_{RF} = 2400\ MHz + RF\_CH\# \cdot 1.0\ MHz + 8MHz\ (Receive\ at\ PIN\#4)$$

      RF_CH #: between 2408MHz and 2524MHz may be set.

Bit 0:

      Set active mode:
            Logic 0: transmit mode
            Logic 1: receive mode

nRF2401 Single Chip 2.4 GHz Radio Transceiver

DATA PACKAGE DESCRIPTION

PRE-AMBLE	ADDRESS	PAYLOAD	CRC

Figure 11 Data Package Diagram

The data packet for both ShockBurst™ mode and direct mode communication is divided into 4 sections. These are:

1. **PREAMBLE**	• The preamble field is required in ShockBurst™ and Direct modes • Preamble is 8 (or 4) bits in length and is dependent of the first data bit in direct mode. PREAMBLE $\quad$ 1st ADDR-BIT $\quad$ 01010101 $\qquad$ 0 $\quad$ 10101010 $\qquad$ 1 • Preamble is automatically added to the data packet in ShockBurst™ and thereby gives extra space for payload. • In ShockBurst™ mode the preamble is stripped from the received output data, in direct mode the preamble is transparent to the output data.
2 **ADDRESS**	• The address field is required in ShockBurst™ mode. • 8 to 40 bits length. • Address automatically removed from received packet in ShockBurst™ mode. In Direct mode MCU must handle address.
3 **PAYLOAD**	• The data to be transmitted • In Shock-Burst mode payload size is 256 bits minus the following: (Address: 8 to 40 bits. + CRC 8 or 16 bits). • In Direct mode the payload size is defined by 1Mbps for 4ms: 4000 bits minus the following: (Preamble: 8 (or 4) bits. + Address: 8 to 40 bits. + CRC: 0, 8 or 16 bits).
4 **CRC**	• The CRC is optional in ShockBurst™ mode, and is not used in Direct mode. • 8 or 16 bits length • The CRC is stripped from the received output data.

Table 18 Data package description

PRODUCT SPECIFICATION

nRF2401 Single Chip 2.4 GHz Radio Transceiver

IMPORTANT TIMING DATA

The following timing applies for operation of nRF2401.

nRF2401 Timing Information

nRF2401 timing	Max.	Min.	Name
PWR_DWN ➔ ST_BY mode	3ms		Tpd2sby
PWR_DWN➔ Active mode (RX/TX)	3ms		Tpd2a
ST_BY ➔ TX ShockBurst™	195µs		Tsby2txSB
ST_BY ➔ TX Direct Mode	202µs		Tsby2txDM
ST_BY ➔ RX mode	202µs		Tsby2rx
Minimum delay from CS to data.		5µs	Tcs2data
Minimum delay from CE to data.		5µs	Tce2data
Minimum delay from DR1/2 to clk.		50ns	Tdr2clk
Maximum delay from clk to data.	50ns		Tclk2data
Delay between edges		50ns	Td
Setup time		500ns	Ts
Hold time		500ns	Th
Delay to finish internal GFSK data		1/data rate	Tfd
Minimum input clock high		500ns	Thmin
Set-up of data in Direct Mode	50ns		Tsdm
Minimum clock high in Direct Mode		300ns	Thdm
Minimum clock low in Direct Mode		230ns	Tldm

Table 19 Switching times for nRF2401

When the nRF2401 is in power down it must always settle in stand-by (Tpd2sby) before it can enter configuration or one of the active modes.
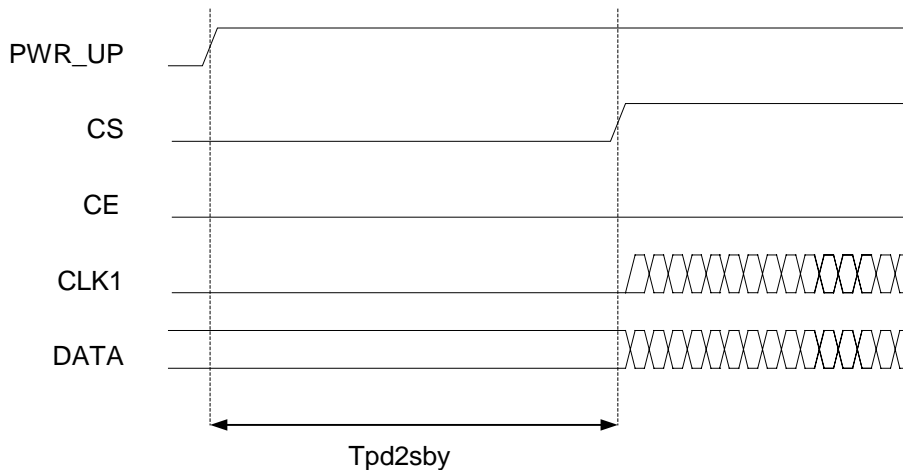

Figure 12 Timing diagram for power down (or VDD off) to stand by mode for nRF2401.

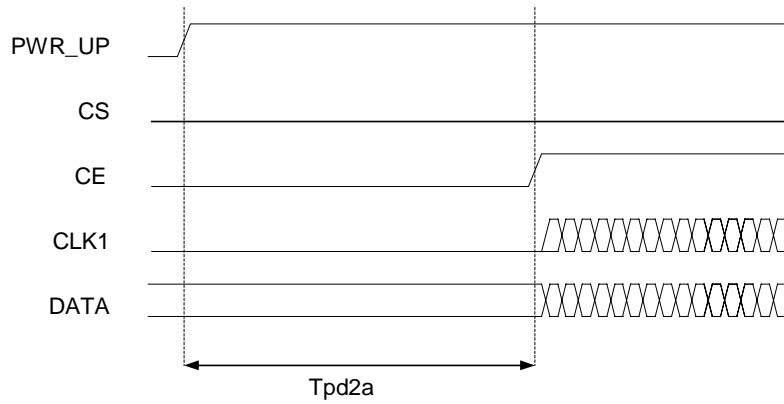**nRF2401 Single Chip 2.4 GHz Radio Transceiver**

Figure 13 Power down (or VDD off) to active mode

Note that the configuration word will be lost when VDD is turned off and that the device then must be configured before going to one of the active modes. If the device is configured one can go directly from power down to the wanted active mode.

Note:

CE and CS may <u>not</u> be high at the same time. Setting one <u>or</u> the other decides whether configuration or active mode is entered.

Configuration mode timing

When one or more of the bits in the configuration word needs to be changed the following timing apply.
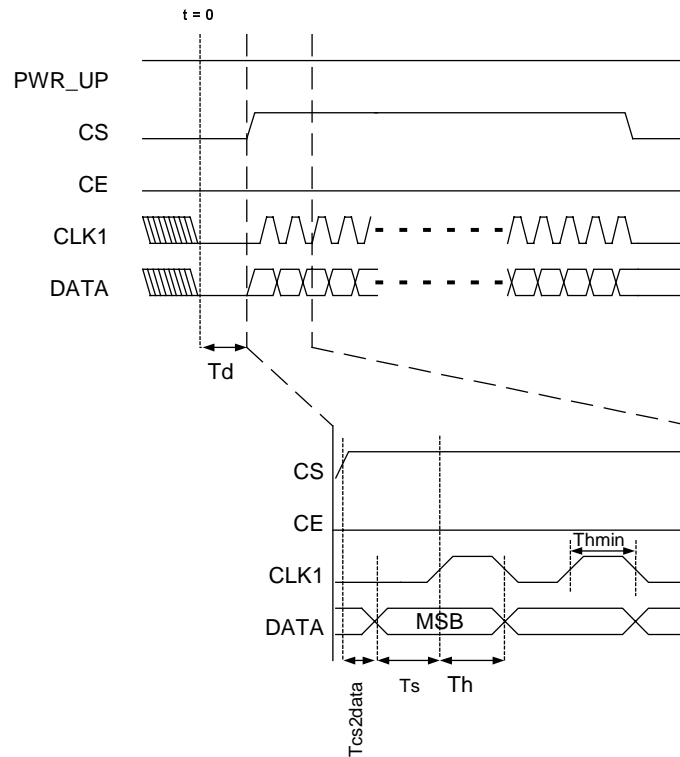
Figure 14 Timing diagram for configuration of nRF2401

If configuration mode is entered from power down, CS can be set high after Tpd2sby as shown in Figure 12.

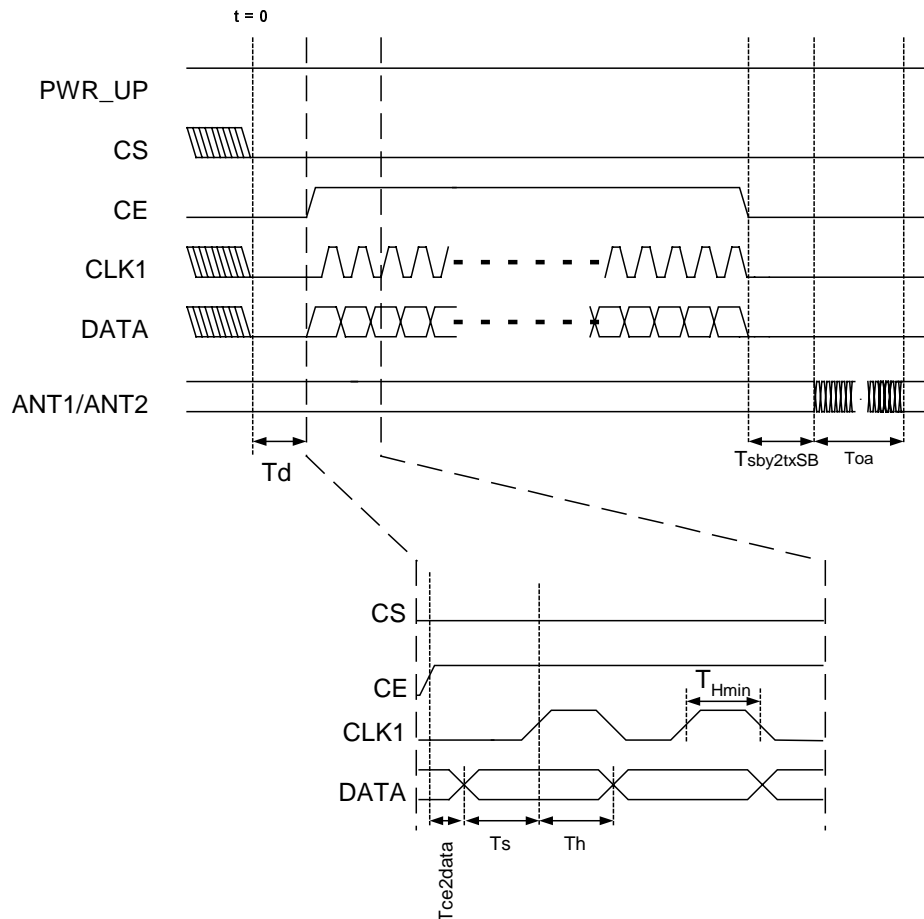## ShockBurst™ Mode timing

ShockBurst™ TX:

Figure 15 Timing of ShockBurst™ in TX

The package length and the data rate give the delay Toa (time on air), as shown in the equation.

$$T_{OA} = 1/datarate \cdot (\#databits + 1)$$
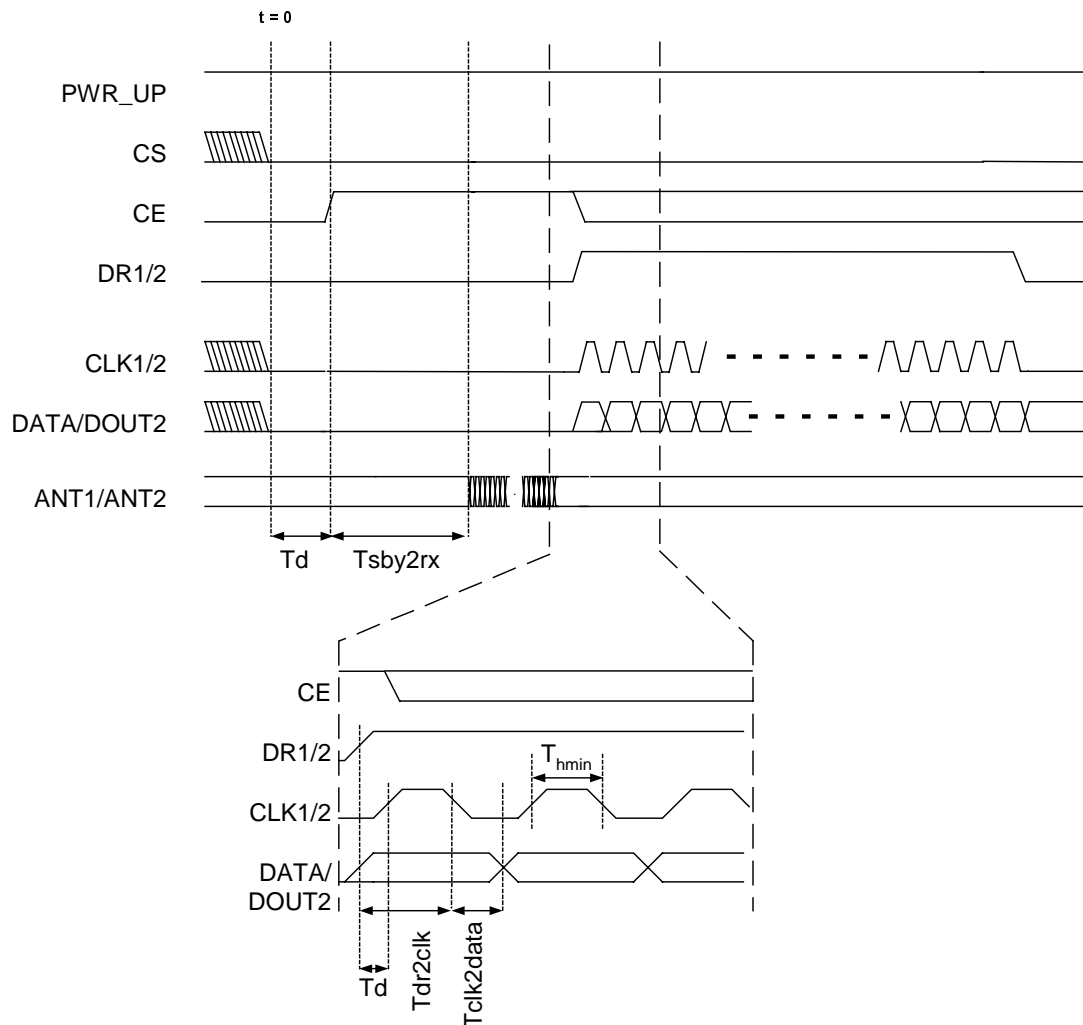
PRODUCT SPECIFICATION

ShockBurst™ RX:

Figure 16 Timing of ShockBurst™ in RX

The CE may be kept high during downloading of data, but the cost is higher current consumption (18mA) and the benefit is no start-up time (200μs) after the DR1 goes low.
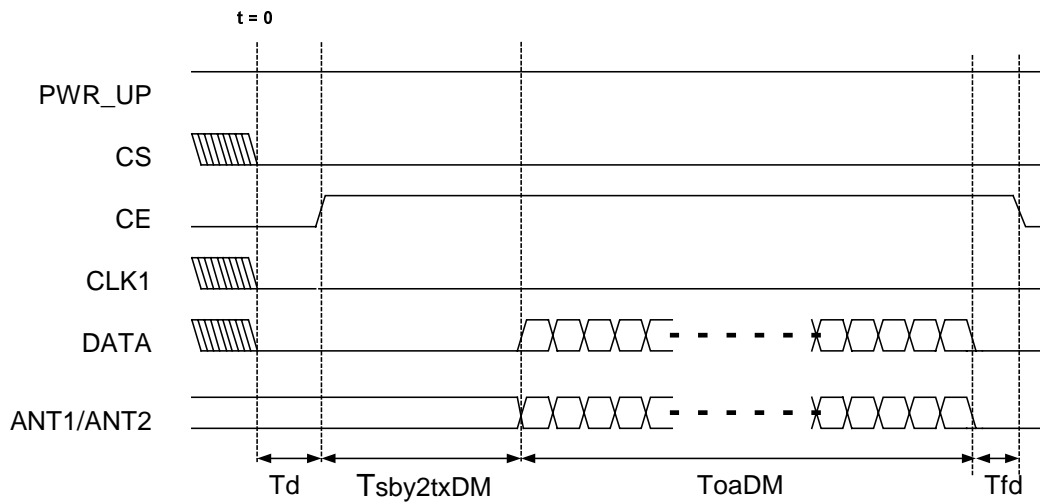
Direct Mode

Direct Mode TX:

Figure 17 Timing of direct mode TX

In TX direct mode the input data will be sampled by nRF2401 and therefore no clock is needed. The clock must be stable at low level during transmission due to noise considerations. The exact delay $T_{sby2txDM}$ is given by the equation:

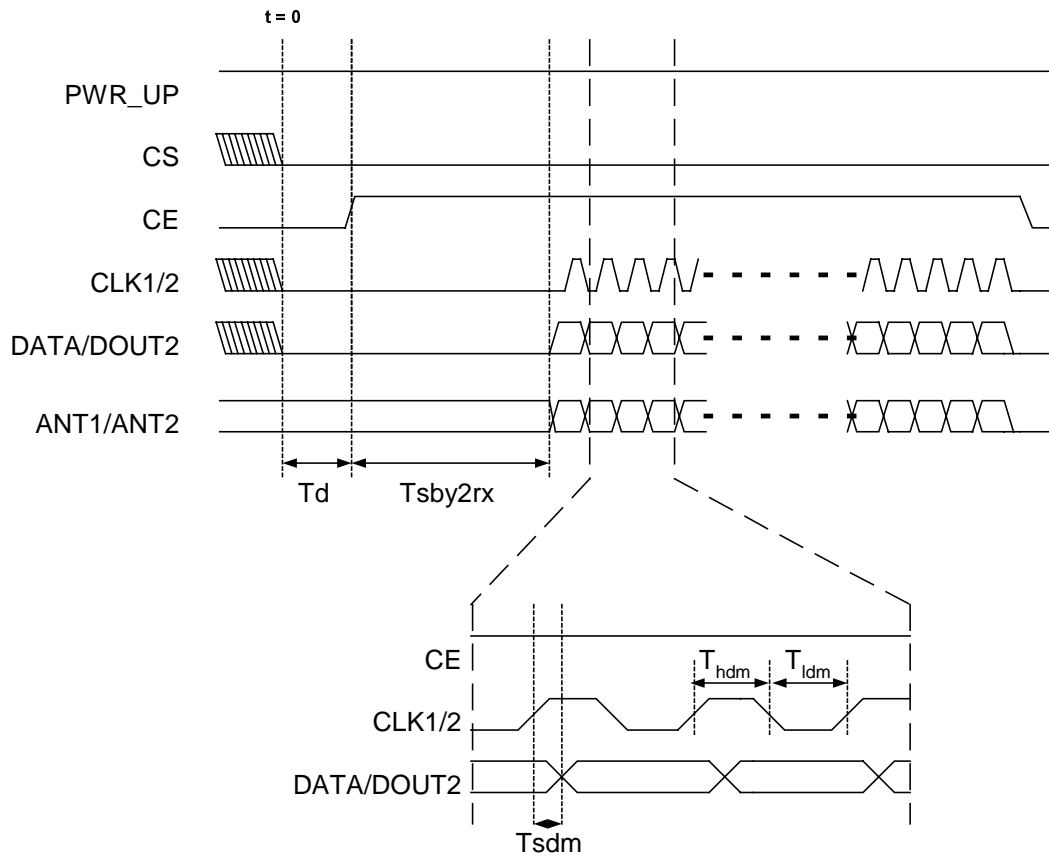$$T_{sby2txDM} = 194us + 1/F_{XO} \cdot 14 + 2.25us$$

Direct Mode RX:

Figure 18 Timing of direct mode RX

Tsby2rx describes the delay from the positive edge of CE to the start detection of (demodulated) incoming data.

PERIPHERAL RF INFORMATION

Antenna output

The ANT1 & ANT2 output pins provide a balanced RF output to the antenna. The pins must have a DC path to VDD, either via a RF choke or via the center point in a dipole antenna. The load impedance seen between the ANT1/ANT2 outputs should be in the range 200-700Ω. A de-embedded load impedance i.e. impedance seen at drain terminals of the output transistors of 400Ω is recommended for maximum output power (0dBm). Lower load impedance (for instance 50 Ω) can be obtained by fitting a simple matching network.

Output Power adjustment

Power setting bits of configuring word	RF output power	DC current consumption
11	0 dBm ±3dB	13.0 mA
10	-5 dBm ±3dB	10.5 mA
01	-10 dBm ±3dB	9.4 mA
00	-20 dBm ±3dB	8.8 mA

Conditions: VDD = 3.0V, VSS = 0V, T_A = 27ºC, Load impedance = 400 Ω.

Table 20 RF output power setting for the nRF2401.

Crystal Specification

Tolerance includes initially accuracy and tolerance over temperature and aging.

Frequency	C_L	ESR	C_{0max}	Tolerance
4	12pF	150 Ω	7.0pF	±30ppm
8	12pF	100 Ω	7.0pF	±30ppm
12	12pF	100 Ω	7.0pF	±30ppm
16	12pF	100 Ω	7.0pF	±30ppm
20	12pF	100 Ω	7.0pF	±30ppm

Table 21 Crystal specification of the nRF2401

To achieve a crystal oscillator solution with low power consumption and fast start-up time, it is recommended to specify the crystal with a low value of crystal load capacitance. Specifying C_L=12pF is OK, but it is possible to use up to 16pF. Specifying a lower value of crystal parallel equivalent capacitance, Co is also good, but this can increase the price of the crystal itself. Typically Co=1.5pF at a crystal specified for Co_max=7.0pF.

PCB layout and decoupling guidelines

A well-designed PCB is necessary to achieve good RF performance. Keep in mind that a poor layout may lead to loss of performance, or even functionality, if due care is not taken. A fully qualified RF-layout for the nRF2401 and its surrounding components, including matching networks, can be downloaded from **www.nvlsi.no**.

A PCB with a minimum of two layers including a ground plane is recommended for optimum performance. The nRF2401 DC supply voltage should be decoupled as close as possible to the VDD pins with high performance RF capacitors, see Table 22. It is preferable to mount a large surface mount capacitor (e.g. 4.7μF tantalum) in parallel with the smaller value capacitors. The nRF2401 supply voltage should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections and VDD bypass capacitors must be connected as close as possible to the nRF2401 IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to have via holes as close as possible to the VSS pads. One via hole should be used for each VSS pin.

Full swing digital data or control signals should not be routed close to the crystal or the power supply lines.

APPLICATION EXAMPLE

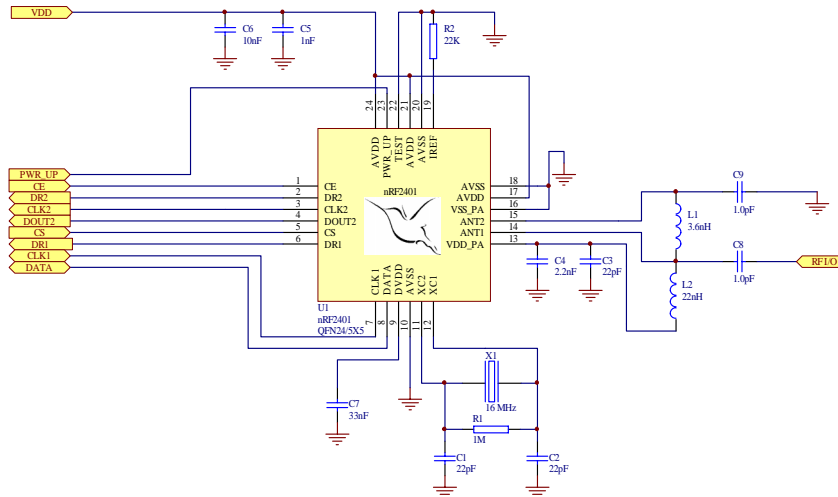## nRF2401 with single ended matching network

Figure 19 nRF2401 schematic for RF layouts with single end 50Ω antenna

Component	Description	Size	Value	Tolerance	Units
C1	Capacitor ceramic, 50V, NPO	0603	22	±5%	pF
C2	Capacitor ceramic, 50V, NPO	0603	22	±5%	pF
C3	Capacitor ceramic, 50V, NPO	0603	22	±5%	pF
C4	Capacitor ceramic, 50V, X7R	0603	2.2	±10%	nF
C5	Capacitor ceramic, 50V, X7R	0603	1.0	±10%	nF
C6	Capacitor ceramic, 50V, X7R	0603	10	±10%	nF
C7	Capacitor ceramic, 50V, X7R	0603	33	±10%	nF
R1	Resistor	0603	1.0	±1%	MΩ
R2	Resistor	0603	22	±1%	KΩ
U1	**nRF2401** transceiver	QFN24 / 5x5	nRF2401		
X1	Crystal, CL = 12pF, ESR < 100 ohm	LxWxH = 4.0x2.5x0.8	16[1]	+/- 30 ppm	MHz
L1	Inductor, wire wound [2]	0603	3.6	± 5%	nH
L2	Inductor, wire wound [2]	0603	22	± 5%	nH
C8	Ceramic capacitor, 50V, NP0	0603	1.0	± 0.25 pF	pF
C9	Ceramic capacitor, 50V, NP0	0603	1.0	± 0.25 pF	pF

Table 22 Recommended components (BOM) in nRF2401 with antenna matching network

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[1] **nRF2401** can operate at several crystal frequencies, please refer to page 31.

[2] Wire wound inductors are recommended, other can be used if their self-resonant frequency (SFR) is > 2.7 GHz

PCB layout example

Figure 20 shows a PCB layout example for the application schematic in Figure 19.

A double-sided FR-4 board of 1.6mm thickness is used. This PCB has a ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. A large number of via holes connect the top layer ground areas to the bottom layer ground plane.
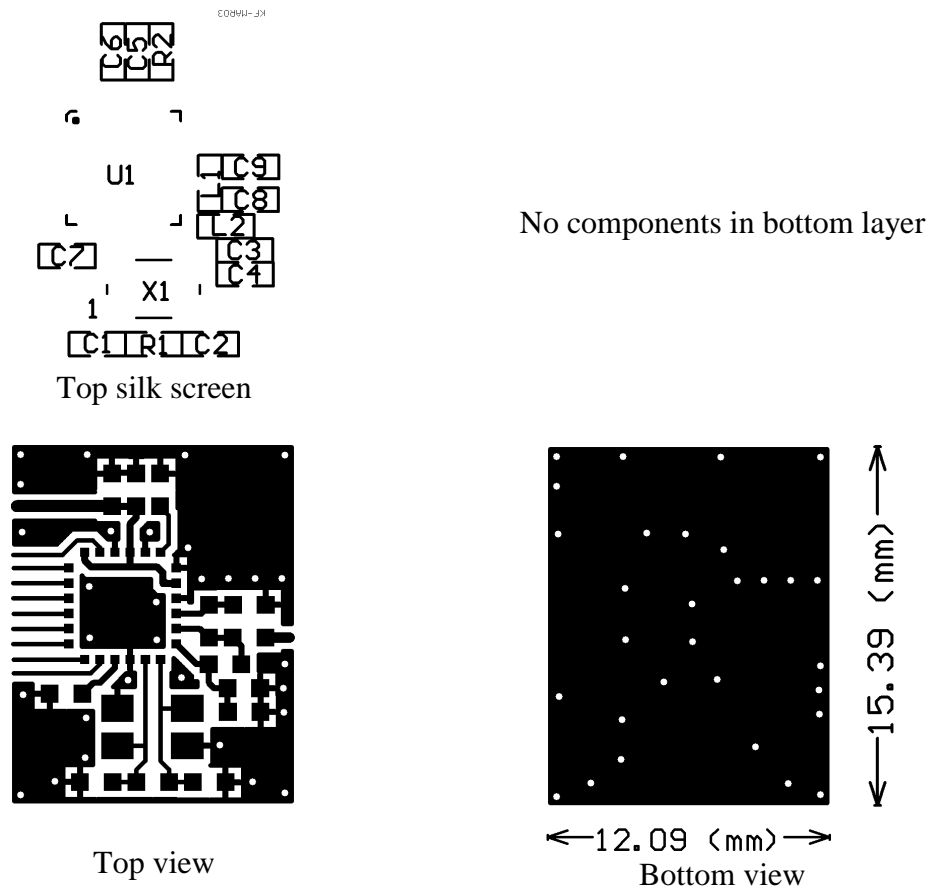
No components in bottom layer

Top silk screen

Top view

Bottom view

12.09 (mm)

15.39 (mm)

Figure 20 nRF2401 RF layout with single ended connection to 50Ω antenna and 0603 size passive components

DEFINITIONS

Data sheet status	
Objective product specification	This datasheet contains target specifications for product development.
Preliminary product specification	This datasheet contains preliminary data; supplementary data may be published from Nordic VLSI ASA later.
Product specification	This datasheet contains final product specifications. Nordic VLSI ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Limiting values	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Table 23. Definitions

Nordic VLSI ASA reserves the right to make changes without further notice to the product to improve reliability, function or design. Nordic VLSI does not assume any liability arising out of the application or use of any product or circuits described herein.

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nordic VLSI ASA customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nordic VLSI ASA for any damages resulting from such improper use or sale.

Preliminary Product Specification: Revision Date: 27.03.2003.

Datasheet order code: 270303-nRF2401.

YOUR NOTES

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